ECIFICATIONS
:
: TSG12864-1186-FFDLWS-R
: NO.1
: _V0
: A1
: TBD
stomer Approved
Date:

Approved	Checked	Designer
	Aron	Sean

- ☐ Preliminary specification for design input
- Full specification for sample approval

RECORDS OF REVISION

Date YYYY/MM DD	Sample Ver.	Spec. Edi.	Description	CHANGED BY	CHECKED BY
2018.10.30	NO.1	V0	First release	Sean	Aron

Contents:

1. SPECIFICATIONS

- 1.1 Features
- 1.2 Mechanical Specifications
- 1.3 Absolute Maximum Ratings
- 1.4 DC Electrical Characteristics
- 1.5 Optical Characteristics
- 1.6 Backlight Characteristics

2. MODULE STRUCTURE

- 2.1 Counter Drawing
- 2.2 Interface Pin Description
- 2.3 Timing Characteristics
- 3. INSPECTION SPECIFICATION

4. RELIABILITY TEST

4.1 Reliability Test Condition

5. PRECAUTION RELATING PRODUCT HANDLING

6.PACKING SPECIFICATION

1. SPECIFICATIONS

1.1 Features

Item	Description
Display Type	128*64 Dots
LCD Type	FSTN /Positive/ Transflective
Driver Condition	1/65 duty, 1/9bais
Viewing Direction	6 O'clock
Backlight Color	White Color
Module weight	About 35.6g
Interface	6800/8080/4SPI
LCD driver IC	ST7565R
ROHS	YES

1.2 Mechanical Specifications

_		-1-2	
	Item	Standard Value	Unit
	Outline Dimension	77.40(L) *52.40(w) *6.50 (H) (Exclude the pin)	mm
	Viewing Area	70.00(L) * 40.00(w)	mm
	Active Area	66.52(L) * 33.24(w)	mm
	Dots Size	0.48(L) *0.48(w)	mm
	Dots Pitch	0.52(L) *0.52(W)	mm

Note: For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
Power Supply Voltage	$V_{ m DD}$	_	-0.3	3.6	V
LCD Power Supply Voltage	VLCD,V0	_	-0.3	13.5	V
LCD Power supply voltage	V1, V2, V3, V4	I	-0.3	V0	V
Any input/output	$V_{\text{IN}}/V_{\text{OUT}}$		-0.3	V _{DD} +0.3	V
Operating Temperature	T_{OP}	ı	-20	70	$^{\circ}$ C
Storage Temperature	T_{ST}		-30	80	$^{\circ}$ C
Storage Humidity	H_D	Ta<40 ℃	-	90	%RH

1.4 DC Electrical Characteristics

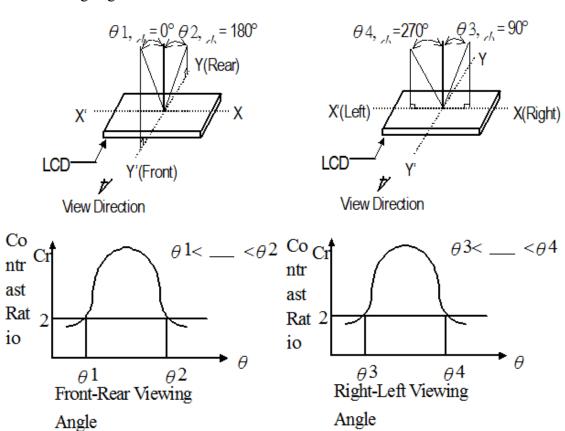
Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Operating Voltage	V_{DD}	-	2.85	3.0	3.15	V
Input High-level Voltage	V _{IHC}	-	0.7Vdd	-	V_{DD}	V
Input Low-level Voltage	V_{ILC}	-	V_{SS}	-	0.3VDD	V
Output High-level Voltage	V _{OHC}	-	$0.8V_{\rm DD}$	-	V_{DD}	V
Output Low-level Voltage	V_{OLC}	-	V_{SS}	-	0.2Vdd	V
LCD Supply Power	V_{LCD}	-	8.8	9.0	9.2	V
Supply Current	I_{DD}	V _{DD} =3.0V,Vop=9.0V, Pattern= Vertical display	-	0.56	0.84	mA

1.5 Optical Characteristics

LCD Panel: 1/65Duty · 1/9Bias · $V_{OP} = 9.0$ V · Ta = 25°C

Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Reference
Response Time		Ton		-	150	250	ma	N-4-2
Kesponse 1	IIIIe	Toff		-	170	300	ms	Note3
	=0(6H)	Y'	C>2.0	20	35	-		
Viewing angle	=90(3H)	X	C <u>></u> 2.0	20	35	-	Dog	Note1
range	=180(12H)	Y		10	25	-	Deg.	Note1
	=270(9H)	X'		20	35	-		
Contrast Ratio		C	$\theta = 0$ °	4	6	-	-	Note2
Average Brightness (with LCD)		IV	VF=3.2V	50	100	-	Cd/m2	NoteA
Uniformity(with LCD)		ΔB		70	75	-	%	Note4

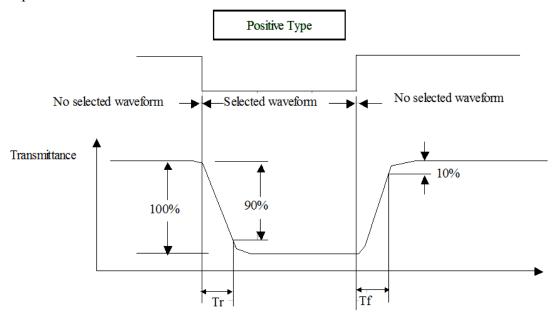
Note 1 Definition of viewing angle

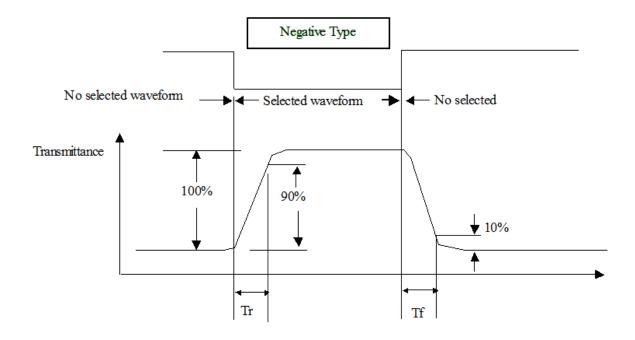


Note 2
Definition of contrast

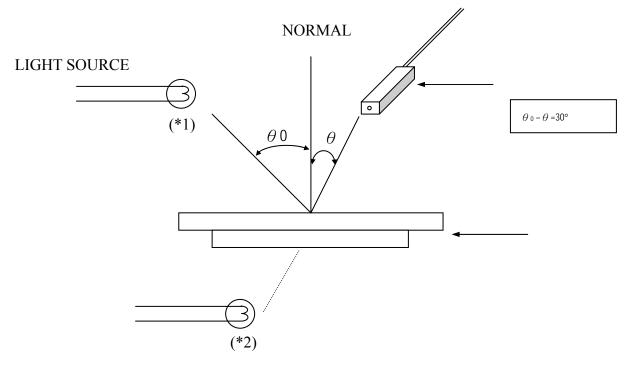
RATIO C.R = Brightness of non-selected segment (B2) Brightness of selected segment Brightness curve of selected segment Brightness curve of non-selected segment Operating voltage (Vop)

Note 3
Definition of response time





Note 4
Measuring Instruments For Electro-optical Characteristics



- *1.Light source position for measuring the reflective type of LCD panel
- *2.Light source position for measuring the transflective / transmissive types of LCD panel

1.6 Backlight Characteristics

LCD Module with LED Backlight

Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25 ℃	-	80	mA
Reverse Voltage	VR	Ta =25°C	-	5.0	V
Reverse Current	IR	VR= 5V	-	40	uA
Power Dissipation	PD	Ta =25 ℃	-	240	mW

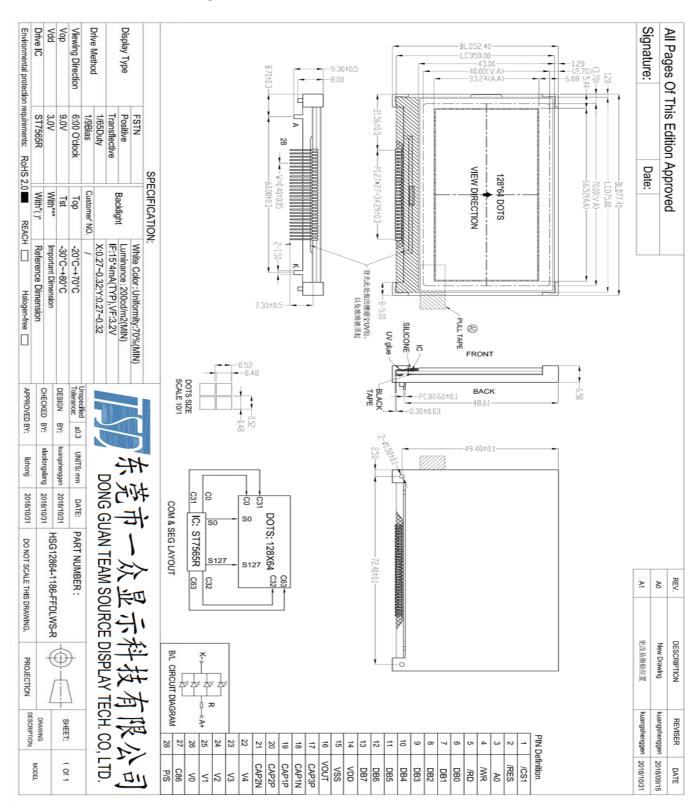
Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Forward Current	IF	VF=3.2V	40	60	80	mA
Average Brightness (without LCD)	IV	VF=3.2V	200	-	-	cd/m ²
Color Coordinates (Without LCD)	Hue	VF=3.2V	X=0.27 Y=0.27	X=0.29 Y=0.29	X=0.32 Y=0.32	nm
Color			White			

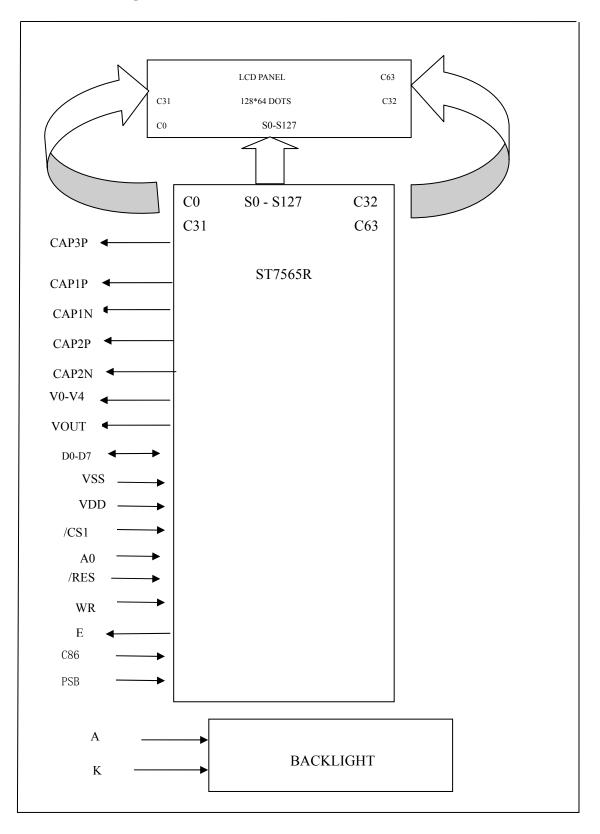
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram



2.1.2 Block Diagram

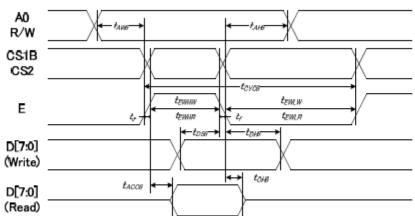


2.2 Interface Pin Description

Pin No.	Symbol	Signal Description			
1	/CS	Chip selection control pin. Low active			
2	/RST	Hardware reset pin. Low active			
3	A0	Command/Data selection control pin.H for display data and L for command data			
4	RW(R/W)	Read/Write signal for 6800 series MPU.			
5	RD(E)	Enable clock input for 6800 series MPU			
6	D0				
7	D1				
8	D2				
9	D3	01;4D; 1; 4; 1,41 D[7.0]			
10	D4	8-bit Bi-direction databus D[7:0].			
11	D5				
12	D6				
13	D7				
14	VDD	Main Power supply for the LCM			
15	VSS	Power Ground			
16	VOUT	DC/DC voltage converter. Connect a capacitor to VDD or VSS			
17	CAP3P	DC/DC voltage converter. Connect a capacitor to CAP3+-			
18	CAP1N	DC/DC voltage converter. Connect a capacitor to CAP1-			
19	CAP1P	DC/DC voltage converter. Connect a capacitor to CAP1+			
20	CAP2P	DC/DC voltage converter. Connect a capacitor to CAP2+			
21	CAP2N	DC/DC voltage converter. Connect a capacitor to CAP2-			
22	V4	V0 power supply for LCD. Connect a capacitor to VSS			
23	V3	V1 power supply for LCD. Connect a capacitor to VSS			
24	V2	V2 power supply for LCD. Connect a capacitor to VSS			
25	V1	V3 power supply for LCD. Connect a capacitor to VSS			
26	V0	V4 power supply for LCD. Connect a capacitor to VSS			
		This is the MPU interface selection pin.			
27	C86	C86 = "H": 6800 Series MPU interface.			
		C86 = "L": 8080 Series MPU interface.			
28	PSB	PSB selects the interface type: Serial or Parallel.			

2.3 Timing Characteristics

System Bus Timing for 6800 Series MPU



(VDD = 3.3V , Ta =25°C)

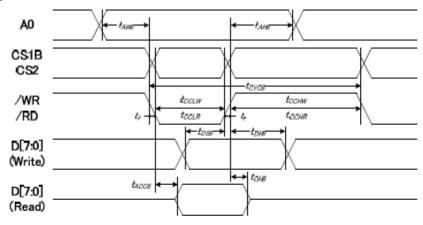
ltem	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	_	
Address hold time	Au	tAH6		0	_	
System cycle time		tCYC6		240	_]
Enable L pulse width (WRITE)		tEWLW		80	_]
Enable H pulse width (WRITE)	E	tEWHW		80	_]
Enable L pulse width (READ)		tEWLR		80	_	ns
Enable H pulse width (READ)		tEWHR		140		
Write data setup time		tDS6		40	_]
Write data hold time	D(7:01	tDH6		10	_]
Read data access time	D[7:0]	tACC6	CL = 100 pF	_	70	
Read data output disable time		tOH6	CL = 100 pF	5	50]

(VDD = 2.7V, Ta =25°C)

ltem	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	40	tAW6		0	_	
Address hold time	A0	tAH6		0	_	
System cycle time		tCYC6		400	_	
Enable L pulse width (WRITE)	7	tEWLW		220	_	
Enable H pulse width (WRITE)	E	tEWHW		180	_	
Enable L pulse width (READ)		tEWLR		220	_	ns
Enable H pulse width (READ)	1	tEWHR		180	_	
Write data setup time		tDS6		40	_	
Write data hold time	D(7:01	tDH6		0	_	
Read data access time	D[7:0]	tACC6	CL = 100 pF	_	140	
Read data output disable time	7	tOH6	CL = 100 pF	10	100	

^{*1} The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.

System Bus Timing for 8080 Series MPU



(VDD = 3.3V, Ta =25°C)

ltem	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	_	
Address hold time	Ć.	tAH8		0	-	
System cycle time		tCYC8		240	_]
/WR L pulse width (WRITE)	WR	tCCLW		80	_]
/WR H pulse width (WRITE)		tCCHW		80	_	
/RD L pulse width (READ)	RD	tCCLR		140	_	ns
/RD H pulse width (READ)	KD	tCCHR		80		
WRITE Data setup time		tDS8		40	_	
WRITE Data hold time	D(7:01	tDH8		20	_]
READ access time	D[7:0]	tACC8	CL = 100 pF	_	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

^{*2} All timing is specified using 20% and 80% of VDD as the reference.

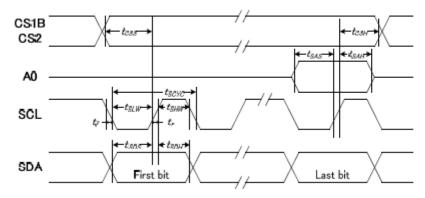
^{*3} tEWLW and tEWLR are specified as the overlap between CS1B being "L" (CS2="H") and E.

(VDD = 2.7V, Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	_	
Address hold time	AU	tAH8		0	_]
System cycle time		tCYC8		400	_]
/WR L pulse width (WRITE)	/WR	tCCLW		220	_]
/WR H pulse width (WRITE)		tCCHW		180	_]
/RD L pulse width (READ)	RD	tCCLR		220	_	ns
/RD H pulse width (READ)	, KD	tCCHR		180	_]
WRITE Data setup time		tDS8		40	_]
WRITE Data hold time	D(7:01	tDH8		0	_	1
READ access time	D[7:0]	tACC8	CL = 100 pF	_	140]
READ Output disable time		tOH8	CL = 100 pF	10	100	

^{*1} The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 - tCCLW - tCCHW) for (tr + tf) ≤ (tCYC8 - tCCLR - tCCHR) are specified.

System Bus Timing for 4-Line Serial Interface



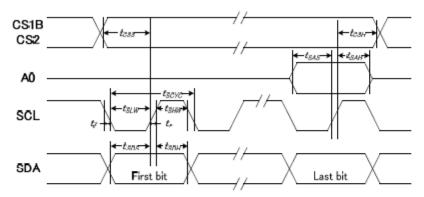
(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period		tSCYC		50	_	
SCLK "H" pulse width	SCLK	tSHW		25	_	
SCLK "L" pulse width		tSLW		25	_	
Address setup time	A0	tSAS		20	_	
Address hold time	AU	tSAH		10	_	ns
Data setup time	SDA	tSDS		20	_	
Data hold time	SDA	tSDH		10	_	
CS-SCLK time	CS1B	tCSS		20	_	
CS-SCLK time	CS2	tCSH		40	_	

^{*2} All timing is specified using 20% and 80% of VDD as the reference.

^{*3} tCCLW and tCCLR are specified as the overlap between CS1B being "L" (CS2="H") and WR and RD being at the "L" level.

System Bus Timing for 4-Line Serial Interface



(VDD = 3.3V, Ta =25°C)

ltem	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period		tSCYC		50	_	
SCLK "H" pulse width	SCLK	tSHW		25	_]
SCLK "L" pulse width		tSLW		25	_]
Address setup time	A0	tSAS		20	_	1
Address hold time	Au	tSAH		10	_	ns
Data setup time	SDA	tSDS		20	_	1
Data hold time	SDA	tSDH		10	_	
CS-SCLK time	CS1B	tCSS		20	_	
CS-SCLK time	CS2	tCSH		40	_	

3. Inspection Specification

AQL inspection standard

Sampling method: GB/T2828.1-2012, Level II, single sampling

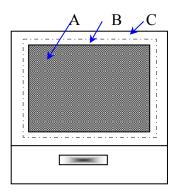
Defect classification:

Classify	Item	Note	AQL
	Short or open circuit		
	LC Leakage		
Major	Display flickering	1	0.65
Major	No display	1	0.63
	Wrong viewing direction		
	Wrong Back-light color		
	Contrast defect(dim,ghost)	2	
	Background color deviation	2	
	black & white spot, dust	3	
	Black, white line defect	4	1.0
Minor	Rainbow	5	1.0
	Chip	6	
	Pin hole	7	
	Cross talk	Refer to sample	

Definition:

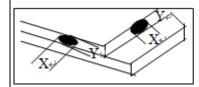
Zone A: Active Area Zone B: Visible Area

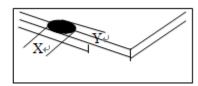
Zone C: outside of Visible Area



No.	Item			Criterion				
	Short or open circuit							
	LC leakage							
	Flickering							
1	No display	Not allowed						
1	Wrong viewing	Not allowed						
	direction							
	Wrong Back-light							
	color							
	Contrast defect							
2	Background color	Refer to approval sa	mple					
	deviation		_					
3	black & white spot, dust(including polarizer). $\phi=(X+Y)/2$	Unit:mm		Ar Point size $\Phi \le 0.1$ $0.1 < \Phi \le 0.15$ $0.15 < \Phi \le 0.2$		Accept QTY A B Any 2 3 0 1		
				Size		eptable (
		- 1	L	W	A	В	C	
	Black, white line	L W	Any	W≤0.01	Any	Any		
4	defect		T .0	0.01 <w≤0.02< td=""><td>2</td><td>4</td><td>An</td></w≤0.02<>	2	4	An	
			L≤2	0.02 <w≤0.03< td=""><td>1</td><td>2</td><td>У</td></w≤0.03<>	1	2	У	
		Unit:mm		0 03 <w< td=""><td>0</td><td>0</td><td></td></w<>	0	0		
			02 ====	or to point defeat				
5	Rainhow				viewine	o area		
5	Rainbow	Unit:mm Remark:While W>0 Not more than two c			viewina	o area		

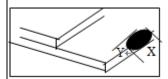
A type and B type :General





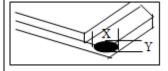
	X	Y	Z
1	Any	≤2.0	≤1/2t
2	≤1/8 X direction glass length	Can not reach the Visible area	≤t

C Type :ITO terminal



X	Y	Z
Any	≤0. 3	≤1/2t
≤1/8X direction (or X≤2)	≰l/5t	≤t

D Type: Corner 1 (on ledge)



Chip

Remark:

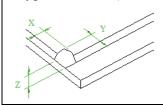
T: glass thickness

X: Notch in X directionY: Notch in Y direction

Z: Notch in Z direction

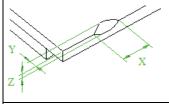
Х	Y	Z
	≤1.5	
≤2	(Can not reach	≤t
	ITO terminal)	

E Type:Corner 2 (beside seal)



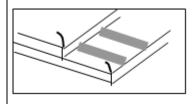
X	Y	Acceptable QTY
≤ 3, 0	Can not	Any
	reach seal	,

F Type :Back of the ITO terminal



Х	Y	Z	Acceptable QTY
≤3. 0	≤1.0	Z≤1/2t	Any

G Tyep:Crack



Can not accept any crack at

anywhere

No.	Item	Criterion		
7	Pin hole	D=(X+Y)/2 X:pin hole length Y:pin hole width d:pattern(segments,dot) width	D D≤1/5d and D≤0.15 D≤1/5d and 0.15 <d<0.2 d="">1/5d or D≥0.2</d<0.2>	Acceptable QTY Any 1 0
8	Total number of acceptable defect	A area(active area) Maximum 2 minor non-conformities per one unit. Defect distance: should be over 10 mm between each point B area(Visible area) It is acceptable when it is no trouble for quality and assembly in customer's end product		

4. RELIABILITY TEST

4.1 Reliability Test Condition

	remaining rest condition		
NO.	TEST ITEM	TEST CONDITION	
1	High Temperature Storage	Keep in 80±2°C 96 hrs	
	Test	Surrounding temperature, then storage at normal condition 4hrs	
2	Low Temperature Storage	Keep in -30±2°C 96 hrs	
	Test	Surrounding temperature, then storage at normal condition 4hrs	
	High Temperature	Endurance test of electrical stress (Voltage & Current) and	
3	Operation	the thermal stress to the elemen	
	Орегация	Keep in 70°C±2°C 96 hrs	
4	Low Temperature	Endurance test of electrical stress (Voltage & Current) and	
	Operation	the thermal stress to the element.	
	Operation	Keep in -20±2°C 96 hrs	
		Keep in +40 °C/90%RH duration for 96 hrs	
5	High Humidity Storage	Surrounding temperature, then storage at normal condition 4hrs(excluding the polarizer)	

6	Thermal shock	-30°C→25°C → 80°C → 25°C	
		(1Hrs) (5mins) (1Hrs) (5mins)	
		10 Cycle	
		Surrounding temperature, then storage at normal condition 4hrs	
7	Vibration Test (Packaged)	1. Sine wave $10 \sim 50$ HZ frequency (1 min)	
		2. The amplitude of vibration :1.5 mm	
		3. Each direction (XYZ) duration for 2 Hrs	

5. PRECAUTION RELATING PRODUCT HANDLING

The following precautions should be followed, since this module contains precise parts.

- (1) Do not store module for an extended periods of time under the conditions of high temperature and high humidity.
- (2) Avoid using or storing the module in areas that expose it to direct sunlight or ultraviolet rays.
- (3) Use protective finger covers when handling the module to avoid scratching or staining the module.
- (4) Care should be taken not to expose the module to static electricity, because the module contains C-MOS LSI's.
 - (5) The LSI is sensitive to light.

 The user's product should be designed so that LSI is not exposed to any light during operation.
- (6) During installation, cover the display area with acrylic protection plates to protect the polarizer plate and LCD cells.
- (7) Do not apply any excessive shocks to the module because the module contains sensitive LCD cells.

Do not use a module, which has experienced strong mechanical shock.

- (8) Care should be taken when the power supply turns on as following.
 - (a) Do not apply any input signals before the supplying voltage is applied.
 - (b) Do not turn off the power supply while any input signals are applied.

Caution

- (1) Dangerous. Do not shock glass because glass can break.
- (2) If module breaks, do not touch it directly.

(Glass could stick or cut skin.)

(3) Do not swallow Liquid Crystal.

(In case of broken LCD panel, do not swallow liquid crystal even if there is no proof that

liquid crystal is poisonous.)

- (4) If liquid crystal is exposed to skin, wash the area thoroughly with alcohol or soap.
- (5) When disposing of the product, please observe industrial waste disposal laws in each country and district.
- (6) In case of injury, give immediate treatment and consult with a doctor.
- (7) This product is constructed precisely. Don't disassemble or modify.
- * Neglecting this mark can cause injury to humans and damage to materials

6.0 PACKING SPECIFICATION

TBD