



深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAYTECH. CO, LTD.

TFT-LCD Module Specification

Module NO.: TST055HDHI-01C

Version: V1.0

☐ APPROVAL FOR SPECIFICATION

☐ APPROVAL FOR SAMPLE

For Customer' s Acceptance:

Approved by	Comment

Team Source Display:

Presented by	Reviewed by	Organized by

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1. GENERAL DESCRIPTION

1.1 DESCRIPTION

TST055HDHI-01C is a transmissive type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT-LCD module (TFT-LCD panel, driver IC and FPC), a back-light unit, and with a CTP. The resolution of **5.5"** contains **720RGB x 1280** pixels and can display up to **16.7M** colors.

1.2 GENERAL INFORMATION

Items	Specification	Unit	Note
Display mode	TFT Transmissive, Positive, NW, IPS	-	-
Drive element	a-Si TFT active matrix	-	-
LCM outline size	71.00(W) x 129.66(H) x 1.62(T)	mm	Note (1)(2)
LCM+CTP size	76.8(W) x 137.4(H) x 2.72(T)	mm	
Active area	68.04(W) x 120.96(H)	mm	-
Number of pixels	720RGB x 1280	pixels	-
Pixel arrangement	RGB stripe	-	-
Pixel size	0.09(W) x 0.09 (H)	mm	-
Display color	16.7M	color	-
Viewing direction	ALL VIEW	-	-
Controller / Driver	ILI9881C	-	-
LCD Data interface	MIPI-4	-	
Backlight	14 White LED,40mA,22.4V	-	
Weight	TBD	g	

Notes:

- (1) Touch panel and back-light unit are included.
- (2) FPC no included. (Refer to the module outline dimension for further information). Please see module specification drawing in **Page8** for more details.

2. ELECTRICAL CHARACTERISTICS

2.1 LCM DC CHARACTERISTICS

(Ta=25±2°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage 2	IOVCC	1.65	1.8	3.3	V	
Power Supply Voltage 3	VCI	2.3	2.8	3.6	V	
Gate Driver High voltage	VGH	9.5	14.25	-	V	
Gate Driver Low voltage	VGL	-6.85	-9.5	-	V	
Current Consumption	I _{DD}	-	TBD	-	mA	Normal mode
	I _{DD-SLEEP}		TBD		uA	Sleep mode
Input voltage "L" Level	V _{IL}	GND	-	0.3IOVCC	V	VDD1=1.65~3.3
Input voltage "H" Level	V _{IH}	0.7IOVCC	-	IOVCC	V	
Output voltage "L" Level	V _{OL}	0	-	0.2IOVCC	V	I _{OL} =1mA
Output voltage "H" Level	V _{OH}	0.8IOVCC	-	IOVCC	V	I _{OH} =-1mA

2.2 BACK-LIGHT UNIT CHARACTERISTICS

The back-light system is an edge-lighting type with **7 chips white LEDs Serial and 2 Parallel connection**. The characteristics of the back-light are shown in the following tables.

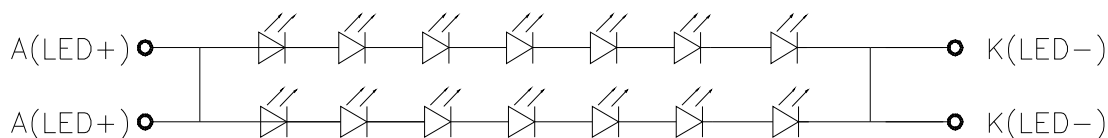
(Ta=25±2°C)

Characteristics	Symbol	Condition	Min.	Type	Max.	Unit	Notes
Forward Voltage	V _f	I _L =40mA	20.3	22.4	23.8	V	
Forward current	I _L		--	40	-	mA	-
Luminance	L _v	I _L =40mA	TBD	TBD	--	cd/m ²	-
LED life time	-	I _L =40mA	10,000	20,000	--	Hr	Note 1

Note:

- (1) The "LED life time" is defined as the module brightness decrease to 50% of original brightness at I_L=40mA. The LED life time could be decreased if operating I_L is larger than 40mA.

Backlight circuit diagram shown in below:



3. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room.

Measuring equipment: BM-5AS, BM-7, EZ-Contrast.

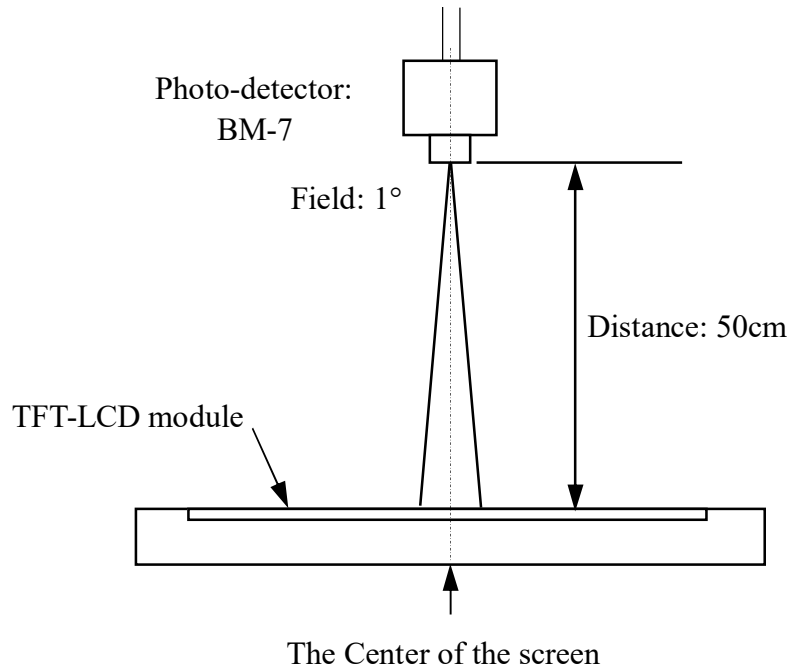
(Ta=25±2°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center point)		C/R	-	500	800	-	-	BM-7 Note(2)
Luminance of white (Center point)		L _w	B/L on	300	350	-	cd/m ²	BM-7
Luminance uniformity		U _w	θ = 0. Normal viewing angle B/L On Note(1)	80	-	-	%	BM-7 Note(3)
Response Time		Tr + Tf		-	25	35	ms	BM-5AS Note(4)
Color Chromaticity (CIE 1931)	White	W _x		0.267	0.297	0.327	-	BM-7 Note(5)
		W _y		0.301	0.331	0.361		
	Red	R _x		0.611	0.641	0.671		
		R _y		0.290	0.320	0.350		
	Green	G _x		0.270	0.300	0.330		
		G _y		0.536	0.566	0.596		
	Blue	B _x		0.104	0.134	0.164		
		B _y		0.098	0.128	0.158		
Viewing Angle	Hor.	θ _L	C/R≥10	80	85	-	Deg	EZ Contrast Note(6)
		θ _R		80	85	-		
	Ver.	θ _u		80	85	-		
		θ _D		80	85	-		
Optima View Direction			ALL VIEW					Note(7)

* This condition will be changed by the evaluation circumstance. If product is exposed to high temperatures for extended time, there is a possibility of the polarizer film damage which could degrade the optical characteristics.

Notes:

- (1) Test Equipment Setup: After stabilizing and leaving the panel alone at a given temperature for 30min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room 30min after lighting the back-light. This should be measured in the center of screen.

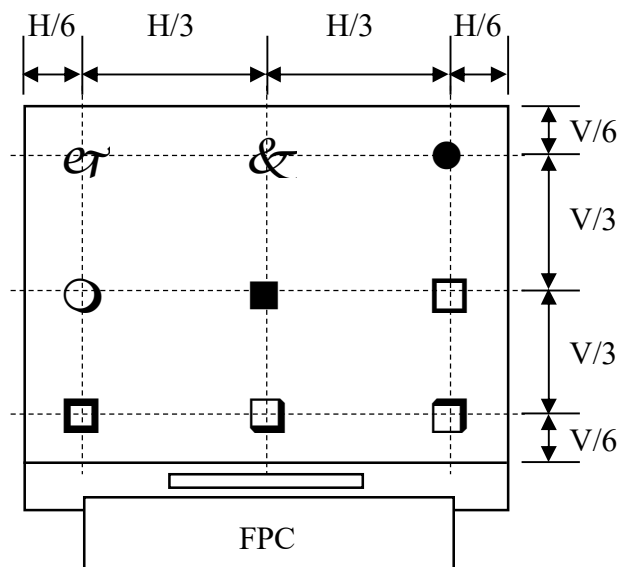


- (2) Definition of Contrast Ratio (CR):

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance measured when LCD on the "white" state}}{\text{Luminance measured when LCD on the "black" state}}$$

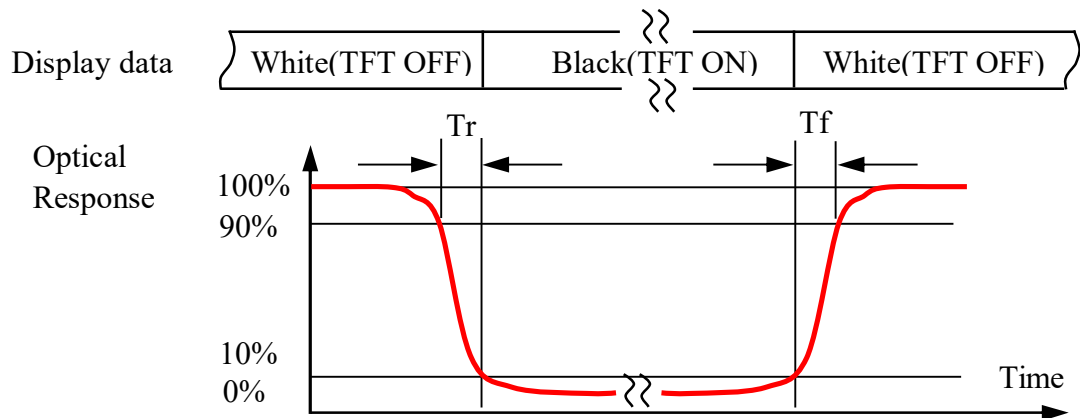
- (3) Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$

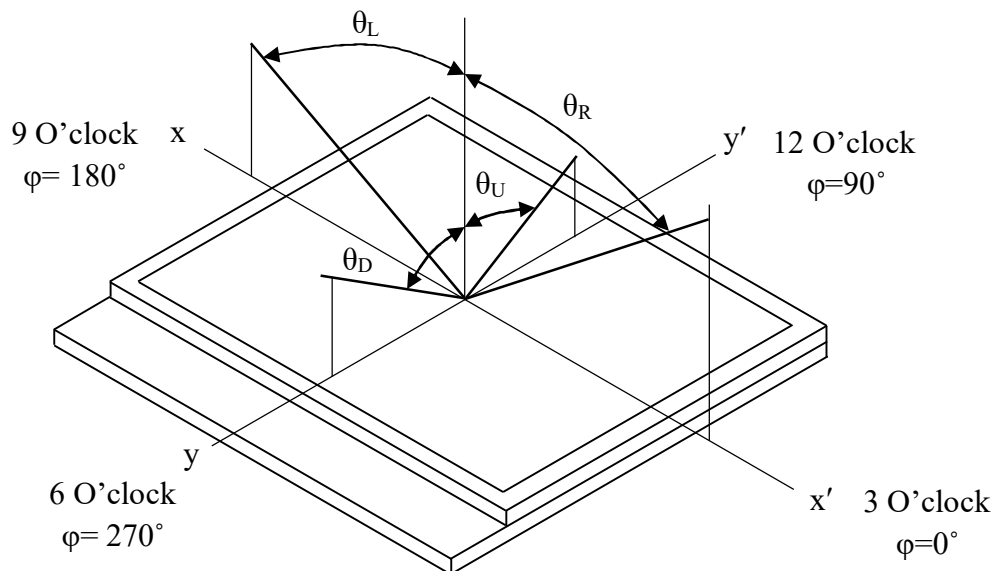


The spot locations for luminance measurement

- (4) Definition of Response time: Sum of T_r and T_f .

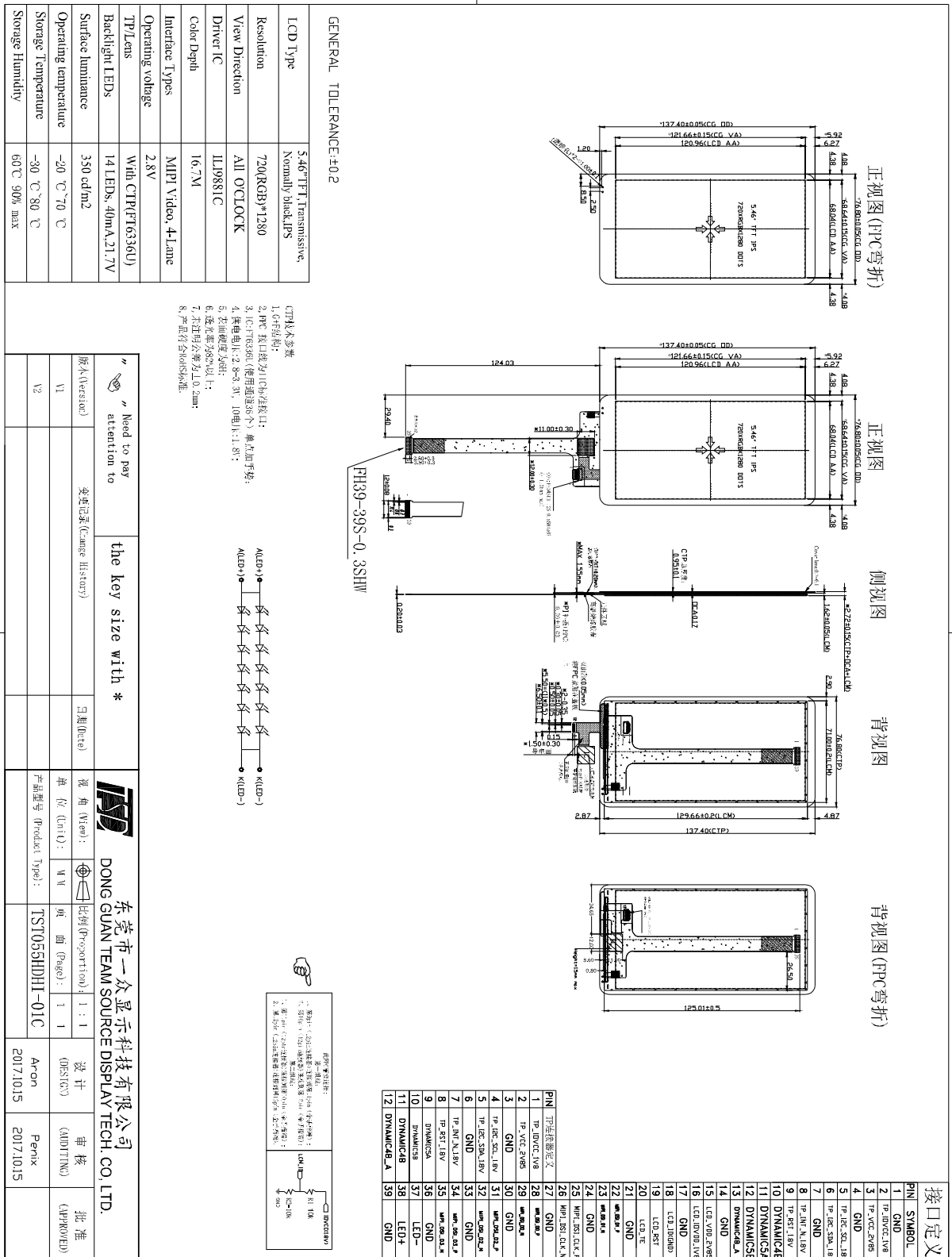


- (5) Definition of Viewing Angle: The viewing angle range that the $CR \geq 10$.



- (6) Definition of Color Chromaticity (CIE 1931)
Color coordinate of white & red, green, blue at center point.
- (7) The different Rubbing Direction will cause the different optima view direction.

4. MODULE OUTLINE DIMENSION



5. MODULE INTERFACE DESCRIPTION

Pin No.	Symbol	I/O	Description	Note
1	GND	P	Ground	
2	TP_1V8	P	Power supply 1.8V	
3	TP_2V85	P	Power supply 2.85V	
4	GND	P	Ground	
5	TP_SCL	I	CTP I ² C clock input	
6	TP_SDA	I/O	CTP I ² C data input/output	
7	GND	P	Ground	
8	TP_INT	O	CTP interrupt signal output pin	
9	TP_RST	I	CTP reset signal input pin	
10	C4B	-	TBD.	
11	C5A	-	TBD.	
12	C5B	-	TBD.	
13	C4B_A	-	TBD.	
14	GND	P	Ground	
15	2V85	P	Power supply 2.85V	2.8V
16	1V8	P	Power supply for I/O interface, 1.8V	1.8V/2.8V
17	GND	P	Ground	
18	ID	P	LCD Identification pin	
19	RST	P	Reset signal	
20	TE	O	Frame Sync signal	
21	GND	P	Ground	
22	D1P	I/O	Data differential signal input pins.(Data lane 1)	
23	D1N	I/O	Data differential signal input pins.(Data lane 1)	
24	GND	P	Ground	
25	CLKP	I/O	Clock differential signal input pins	
26	CLKN	I/O	Clock differential signal input pins	
27	GND	P	Ground	
28	D0P	I/O	Data differential signal input pins.(Data lane 0)	
29	D0N	I/O	Data differential signal input pins.(Data lane 0)	
30	GND	P	Ground	
31	D2P	I/O	Data differential signal input pins.(Data lane 2)	
32	D2N	I/O	Data differential signal input pins.(Data lane 2)	
33	GND	P	Ground	
34	D3P	I/O	Data differential signal input pins.(Data lane 3)	
35	D3N	I/O	Data differential signal input pins.(Data lane 3)	
36	GND	P	Ground	
37	LEDK	P	Back-light Cathode	

38	LEDA	P	Back-light Anode	
39	GND	P	Ground	

6. REFERENCE APPLICATION CIRCUIT

Please consult our technical department for detail information.

7. TIMING DIAGRAM

7.1 RESET TIMING CHARACTERISTICS

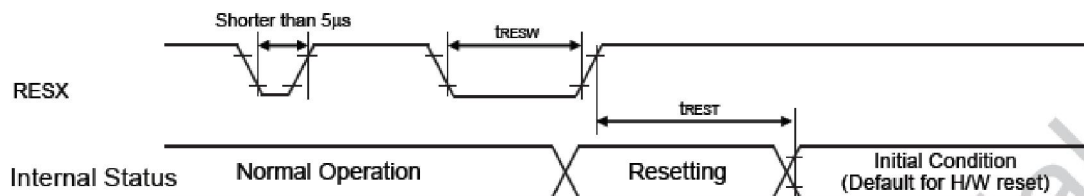


Table 7.3.2.1 Reset input timing

VSS=0V, VDDIO=1.8V to 3.6V, VCI=2.5V to 5.5V, Ta = -30 to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

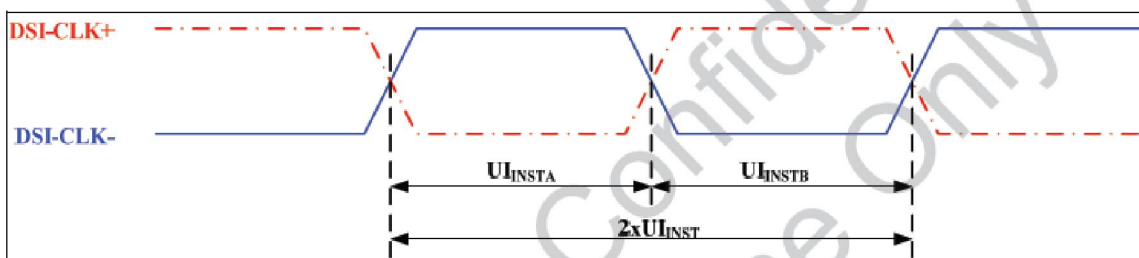
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

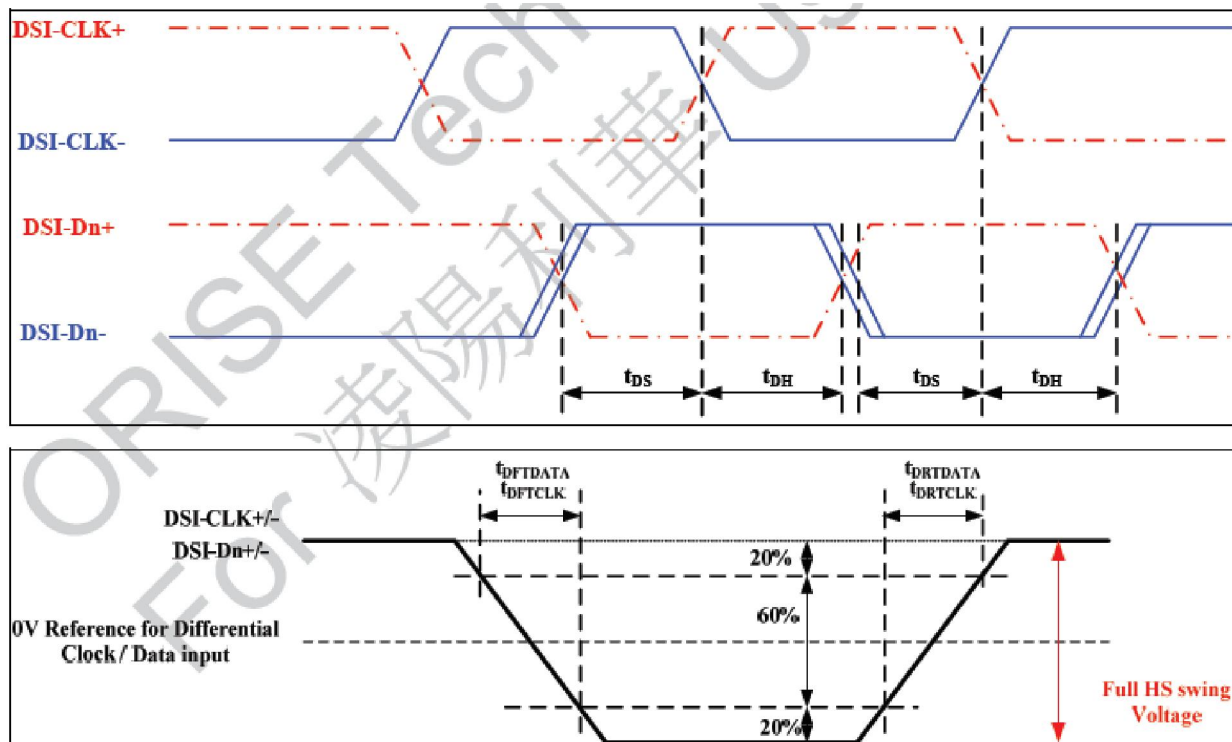
RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset starts (It depends on voltage and temperature condition.)

7.2 MIPI-DSI CHARACTERISTICS

7.2.1 HIGH SPEED CYCLE SEQUENCE

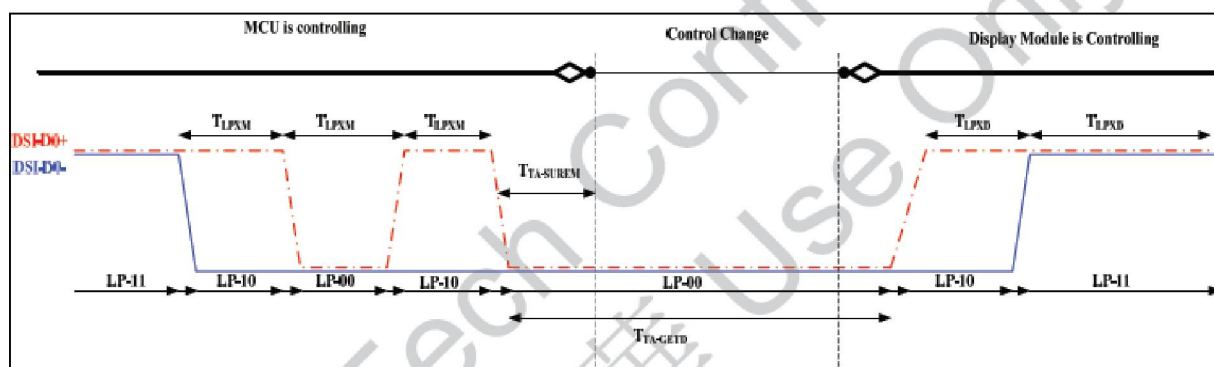
Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed mode						
DSI-CLK+/-	2xUI _{INST}	Double UI instantaneous	4	-	25	ns
DSI-CLK+/-	UI _{INSTA} , UI _{INSTB}	UI instantaneous Halfs	2	-	12.5	ns
DSI-Dn+/-	t _{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t _{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t _{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DRTDATA}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t _{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DFTDATA}	Differential fall time for data	150	-	0.3UI	ps





7.2.2 LOW POWER CHARACTERISTICS

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T _{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	-	ns
DSI-D0+/-	T _{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	58	-	-	ns
DSI-D0+/-	T _{TA-SURED}	Time-out before the MPU start driving	T _{LPXD}	-	2XT _{LPXD}	ns
DSI-D0+/-	T _{TA-GETD}	Time to drive LP-00 by display module	5XT _{LPXD}	-	-	ns
DSI-D0+/-	T _{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4XT _{LPXD}	-	-	ns
DSI-D0+/-	Ratio T _{LPX}	Ratio of T _{LPXM} / T _{LPXD} between MCU and display module	2/3	-	3/2	



8. Capacitive Touch Panel specifications

8.1 Mechanical characteristics

DESCRIPTION	INL SPECIFICATION	REMARK
Touch Panel Size	5.5	
Outline Dimension (OD)	76.8(H) x 137.4(V)x mm	Cover Lens Outline
Product Thickness	1.67mm(max)	
Glass Thickness	0.7mm	
Ink View Area	68.64x121.66mm	
Input Method	1 Fingers + gesture(单点+手势)	
Activation Force	Touch	
Surface Hardness	≥6H	

8.2 Electrical characteristics

DESCRIPTION		SPECIFICATION
Operating Voltage		DC 2.8~3.6V
Power Consumption (IDD)	Active Mode	12~4.5mA
	Sleep Mode	TBD
Interface		I ² C
Controller IC		FT6336U
I ² C address		0x70
Resolution		720*1280

8.3 Interface timing characteristics

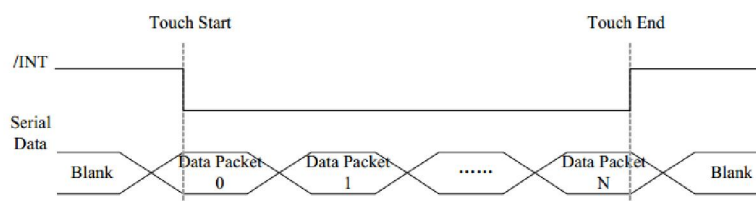
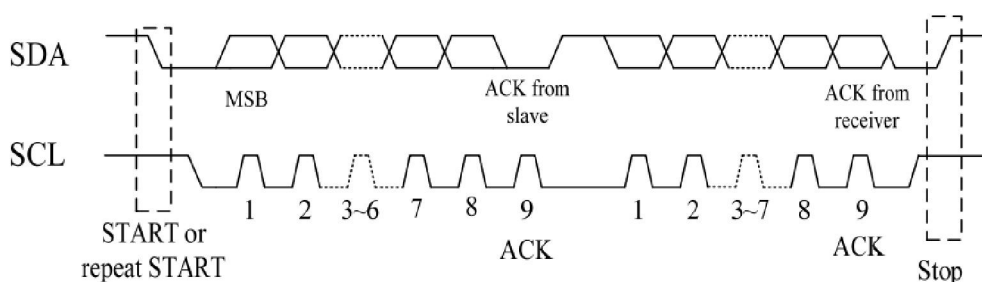


Figure 1-2 Interrupt query mode

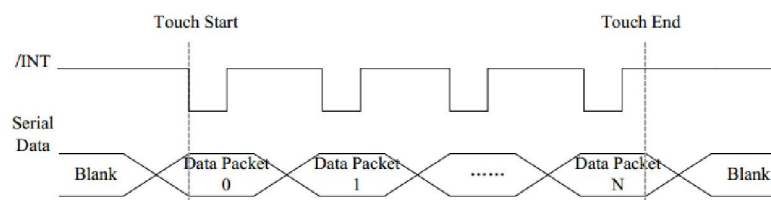
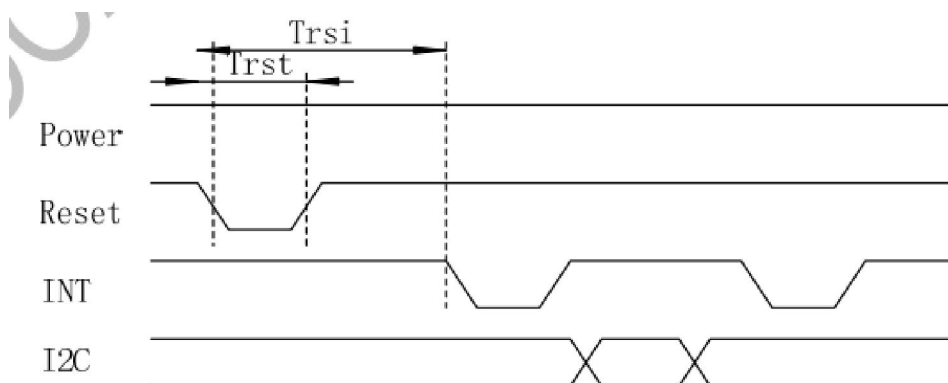
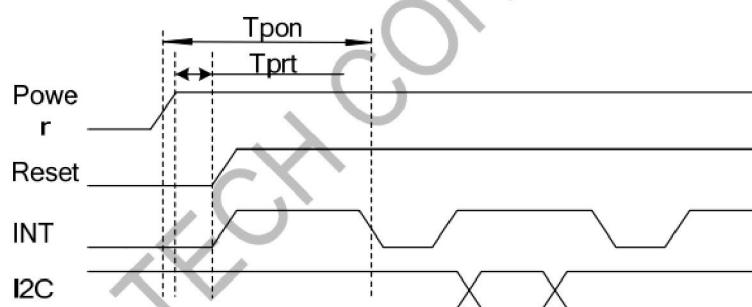


Figure 1-3 Interrupt trigger mode

PARAMETER	MIN	MAX	UNIT
SCL Frequency	10K	400K	Hz
Bus Free Time Between a STOP and START Condition	4.7	-	uS
Hold Time (repeated) START Condition	4.0	-	uS
Data Setup Time	250	-	nS
Setup Time for Repeated START Condition	4.7	-	uS
Setup Time for STOP Condition	4.0	-	uS

8.4 Power on/Reset/Wake Sequence Parameters



Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

9. RELIABILITY TEST CONDITIONS

No.	Test Item	Test Condition	Notes
1	High Temperature Storage	+80°C / 120H	Inspection after 2~4h storage at room temperature, the sample shall be free from defects: 1. Air bubble in the LCD; 2. Seal leak; 3. Non-display; 4. Missing segments; 5. Glass crack; 6. The surface shall be free from damage. 7. The electrical characteristics requirements shall be satisfied.
2	Low Temperature Storage	-30°C / 120H	
3	High Temperature Operating	+70°C / 120H	
4	Low Temperature Operating	-20°C / 120H	
5	Temperature Cycle	-20±2°CΔ25°CΔ+70±2°C x 10cycles (30min) (5min) (30min)	
6	High Temperature /Humidity storage	50+5°C x 90%RH / 120H	
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z	
8	Packing Drop Test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	
9	ESD test	Voltage:±8KV R: 330Ω C: 150pF Air discharge, 10time	

Remarks:

- (1) The test samples should be applied to only one test item.
- (2) Sample size for each test item is 5~10pcs.
- (3) For High Temperature/Humidity storage test, pure water (resistance>10MΩ) should be used.
- (4) In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
- (5) Failure judgment criterion: basic specification, electrical characteristic, mechanical characteristic, optical characteristic.

10. PACKING SPECIFICATION

TBD.